IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/630,332	Confirmation No.: 8758
Appellant:	Hyesook Hong	
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Examiner:	Ron Everett Pompey	
Docket:	TI-35165	
Customer No.:	23494	

CORRECTED APPEAL BRIEF

March 9, 2011

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Corrected Appeal Brief filed pursuant to the Notice of Non-compliant Appeal Brief dated 2/11/2011. Only the corrected section is included below.

Summary of Claimed Subject Matter under 37 C.F.R. §41.37(c)(1)(v)

The invention of Claim 9 is a method for monitoring critical dimension (CD) variations of a reticle 100. Referring to FIGURE 1, a reticle layer 110 is provided over a reticle substrate (para. [0018]) and includes each of: a patterned feature area 120a/120b corresponding to a desired circuitry pattern (para. [0021]); and a test pattern area 130a/130b, wherein a portion of the test pattern area is within a step-distance of a

portion of the patterned feature area (para. [0024]). Referring to FIGURE 3, a resist material is patterned by stepping the reticle, the patterning including each of the patterned feature area and test pattern area incorporated in the reticle layer (para. [0038]). The resist material is visually inspected for light and dark regions within the test pattern area, where the light and dark regions represent a corresponding variance in the patterned feature area of the resist material (para. [0034] and [0040]). Using the resist material as patterned by the reticle, the feature of a semiconductor device is formed after the visually inspecting step (para. [0042]).

A key to the invention is recognizing that variances in a pattern feature area can be made to appear as light and dark regions in a specially designed test pattern. The light and dark regions of the invention, an example of which is shown in FIG 3, are at a more macro view (viewing multiple step regions) than at a more micro view (individual elements similar to FIG. 2). A variance is shown in FIG. 3 as one block 320 appearing as a lighter shade of grey (light region) that another block 330 (dark region). Each block corresponds to a step area (para. [0033]-[0034]). The variance in FIG. 3 appears as blocks of various shades of grey (i.e., the light and dark regions) rather than the black and white of a micro view.

The invention of Claim 10 further requires that a first portion 130a of a test pattern area is within a step-distance of a first portion 120a of a patterned feature area and a second portion 130b of a test pattern area is within a step-distance of a second portion 120b of a patterned feature area (FIG 1). A variance between the first and second portions of the test pattern area is indicative of a variance between the first and second portions of the patterned feature area (para [0024]-[0025]).

The invention of Claim 11 further requires that the test pattern area creates a reflective grating in the patterned resist material wherein the reflective grating is

configured to provide the light and dark regions if the variance in the patterned feature area exists (para [0029]).

The invention of Claim 18 is a method for making a semiconductor device. Referring to FIGURE 3, a resist material is patterned by stepping the reticle 100. Each reticle includes a patterned feature area 120a/120b corresponding to a desired feature of a semiconductor device and a test pattern area 130a/130b, wherein a portion of the test pattern area is within a step-distance of a portion of the patterned feature area (paragraph [0024] and FIGURE 1). The patterned resist layer is visually inspecting for light and dark regions within a corresponding test pattern area, said light and dark regions representing a systematic variance in critical dimension (CD) in said patterned resist material (paragraphs [0034] and [0040]). Using the resist material as patterned by the reticle, the feature of a semiconductor device is formed after the visually inspecting step (para. [0042]).

The invention of claim 21 is a method for making a semiconductor device by patterning a resist material using a reticle 100 having a plurality of step areas A-X within the reticle (paragraph [0020]). As shown in FIGURE 1, the reticle includes a patterned feature area 120a/120b corresponding to a desired feature of a semiconductor device and a test pattern area 130a/130b, wherein a portion of the test pattern area is within a step-area distance of a portion of the patterned feature area (paragraph [0024]). The patterned resist material is visually inspected for light and dark regions, differences in the light and dark regions between the plurality of step areas representing a systematic variance in critical dimension (CD) in the patterned resist material paragraph [0034] and [0040]). The patterned resist material is used to form the feature of a semiconductor device after visually inspecting (paragraph [0042], step 480 of Figure 4).

Respectfully submitted,

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